IN THE CLAIMS:

1-17 (Cancelled)

18. (New) A semiconductor memory element comprised of:

a plurality of word lines;

a plurality of data lines; and

memory cells at the intersections of the word lines and data lines, each memory cell being comprised of

a storage transistor with a gate terminal electrically connected to a storage node and one of a source or drain region connected to a predetermined potential,

a read transistor with a gate terminal electrically connected to a read word line and a source or drain region connected to the other one of said ~~a~~ source or drain region of the storage transistor and the other one of the source or drain region of the read transistor connected to one of the data lines, and

a semiconductor write device with a gate terminal electrically connected to a write word line and one of a source or drain region of the write device connected to a second one of said data lines and the other one of the source or drain region of the write device connected to the storage node, wherein said semiconductor write device source region and drain region are fabricated from metal or a semiconductor material connected by a channel which is formed by a semiconductor material with a thickness of no more than 5 nanometers on top of an insulating film, wherein said one side surface of said channel is substantially located on a same plane as said source region and drain region, and another side surface of said channel is located in different plane from said source region and drain region.

19. (New) A semiconductor element according to Claim 18, further comprising a plurality of sense amplifiers, wherein one of said sense amplifiers is connected to each data line to amplify a signal during a read operation.

20. (New) A semiconductor element according to Claim 19, wherein the storage transistor is an N-channel MOS device.

21. (New) A semiconductor element according to claim 20, wherein a refresh operation is conducted in a manner such that a signal on a read data line is amplified and applied to a write data line through a pass transistor, followed by the activation of the write transistor to store the data.

22. (New) A semiconductor element according to Claim 20, wherein a write data line and a read data line are connected via transistor.

23. (New) A semiconductor element according to Claim 22, wherein a refresh operation is conducted in such a manner that the signal on a data line is amplified, followed by the activation of the write transistor to store the data.

24. (New) A semiconductor memory element, comprised of:

a plurality of word lines;

a plurality of data lines; and

memory cells at the intersections of the word lines and data lines, each of said memory cells comprising

a storage transistor with a gate terminal electrically connected to a storage node and one of a source or drain region connected to a predetermined potential,

a semiconductor write transistor activated by a write word line electrically connected to the storage node wherein one of a source or drain region of the semiconductor write transistor is connected to one of the data lines and the other one of the source or drain region of the semiconductor write transistor is connected to the storage node, wherein said semiconductor write ~~device~~ transistor ~~has a~~ source region and drain region are fabricated from a conductor connected by a channel which is formed by a semiconductor material of a thickness of no more than 5 nanometers on top of an insulating film, further wherein a first side surface of said channel is substantially located on a same plane as said source region and drain region of said write transistor, and a second side surface of said channel is located in a different plane from said source region and drain region of said write transistor.

25. (New) A semiconductor memory element according to Claim 24, wherein said conductor is a metal or a semiconductor material.

26. (New) A semiconductor memory element according to Claim 25, wherein the source or drain of the write transistor that is electrically connected to the gate terminal of the storage transistor is formed from a single body of polysilicon.

27. (New) A semiconductor memory element according to Claim 26, wherein the polysilicon gate terminal of the storage transistor has ~~an~~ first conductivity type impurity and the polysilicon source and drain region of the write transistor has ~~an~~ second conductivity type impurity which is of the opposite type from said first conductivity type.

28. (New) A semiconductor memory element according to Claim 25, wherein the upper part of the polysilicon drain and source regions of the write transistor has a higher concentration of impurities than the lower part of the polysilicon drain and source regions.

29. (New) A semiconductor memory element according to Claim 25, wherein a vertical stack comprising of a layer of polysilicon with one type of doping, a layer of metal or silicide, and a layer of polysilicon of the opposite type of doping is used in a manner such that the lower part of the stack is the gate terminal of the storage transistor and the upper part of the stack is the source or drain region of the write transistor.

30. (New) A semiconductor memory element according to Claim 25, wherein one of the source or drain of the write transistor is fabricated vertically above the source or drain of the storage transistor, and further wherein these two vertically oriented terminals are connected electrically by a contact between the two terminals.

31. (New) A semiconductor memory element, comprised of:

a plurality of word lines;

a plurality of data lines; and

memory cells at the intersections of the word lines and data lines, each of said memory cells comprising

a storage transistor with a gate terminal electrically connected to a storage node and one of a source of drain region connected to a predetermined potential, and

a semiconductor write device activated by a write word line electrically connected to the gate terminal of the write device and one of a source or drain region of the semiconductor write device is connected to one of the data lines and the other one of the source or drain region of the semiconductor write device is-connected to the storage node;

wherein said semiconductor write device source region and drain region are fabricated from metal or a semiconductor material connected by a channel which is formed by a semiconductor material with a thickness of no more than 5 nanometers on top of an insulating film, wherein one side surface of said channel is substantially located on a same plane as said source region and drain region of the write device, and a second side surface of said channel is located in a different plane from said source region and drain region of the write device;

wherein each of a pair of memory cells is connected to a separate data line and further wherein the source or drain regions of the semiconductor write devices of each of the pair of memory cells that are not connected to the storage nodes in the respective cells are electrically connected.

32. (New) A semiconductor memory cell, comprising:

a first switch element, and

a first capacitor element, wherein a first terminal of the first capacitor element is electrically connected to a first terminal of the first switch element at a storage node, and a second terminal of the first capacitor element is connected to a reference potential, wherein said first switch element is adapted to transfer a charge to the storage node based on a voltage of an external data line, and the storage node is coupled to said external data line by capacitive coupling and

further said external data line is adapted to obtain at least two voltage values Vd1 and Vd2, wherein said Vd1 > Nd2 and, during a write operation to the memory cell, the charge stored at the storage node is Qs1 when a voltage of the external data lines is Vd1, and Qs2 when a voltage of the external data lines is Vd2, and wherein said Qs1 is smaller than saidQs2,

and wherein said switch element has a source region and drain region fabricated from metal or a semiconductor material connected by a channel which is formed by a semiconductor material with a thickness no more than 5 nanometers on top of an insulating film, wherein one side surface of said channel is substantially

located on a same plane as said source region and drain region of said switch element and a second side surface of said channel is located in a different plane from said source region and drain region.

33. (New) A semiconductor memory element comprised of:

a plurality of read and write word lines;

a plurality of read and write data lines; and

memory cells at the intersections of the word lines and data lines, each memory cell being comprised of

a storage transistor with a gate terminal electrically connected to a storage node and one of a source or drain region connected to a predetermined potential,

a read transistor with a gate terminal electrically connected to a read word line and a source or drain region connected to the other one of said source or drain region of the storage transistor and the other one of the source or drain region of the read transistor connected to a read data line, and

a semiconductor write transistor with a gate terminal electrically connected to a write word line and one of a source or drain region of the write transistor connected to a write data line and the other one of the source or drain region of the write transistor connected to the storage node, wherein said semiconductor write transistor source region and drain region fabricated from metal or a semiconductor material connected by a channel which is formed by a semiconductor material with a thickness of no more than 5 nanometers on top of an insulating film, wherein one side surface of said channel is substantially located on a same plane as said source region and drain region of the write transistor, and a second side surface of said channel is located in a different plane from said source region and drain region of the write transistor.

34. (New) A semiconductor element according to Claim 33, further comprising a plurality of sense amplifiers, wherein one of said sense amplifiers is connected to each read data line to amplify a signal during a read operation.